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1 A survey of Boolean matching techniques for library binding
Luca Benini, Giovanni De Micheli
July 1997 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 2 Issue 3
Publisher: ACM Press
Full text available: pdf(321.93 KB) Additional Information: full citation, abstract, references, citings, index terms

When binding a logic network to a set of cells, a fundamental problem is recognizing whether a cell can implement a portion of the network. Boolean matching means solving this task using a formalism based on Boolean algebra. In its simplest form, Boolean matching can be posed as a tautology check. We review several approaches to Boolean matching as well as to its generalization to cases involving don't care conditions and its restriction to specific libraries such as those ...

2 Boolean matching for large libraries
Uwe Hinsberger, Reiner Kolla
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(434.77 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Boolean matching tackles the problem whether a subcircuit of a boolean network can be substituted by a cell from a cell library. In previous approaches [7, 10, 8] each pair of a subcircuit and a cell is tested for NPN equivalence. This becomes very expensive if the cell library is large. In our approach the time complexity for matching a subcircuit against a library L is almost independent of the size of L. CPU time also remains small for matching a subcirc ...

Keywords: emulation, functional simulation, reconstruction, visibility

3 Generalized matching from theory to application
Patrick Vuillod, Luca Benini, Giovanni De Micheli
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf(252.57 KB)

Publisher Site Additional Information: full citation, abstract, references, index terms

We present a novel approach for post-mapping optimization. We exploit the concept of generalised matching, a technique that finds symbolically all possible matching assignments of library cells to a multi-output network specified by a Boolean relation. Several objectives are targeted: area minimization under delay constraints; power minimization under delay constraints; and unconstrained delay minimization. We describe the theory of generalized matching and the algorithmic optimization required ...

Keywords: Boolean relation, MCNC 91 benchmark suite, algorithmic optimization, area minimization, delay constraints, generalized matching, library cells, logic CAD, multi-output network, post-mapping optimization, power minimization, unconstrained delay minimization

4 Boolean matching for incompletely specified functions

Kuo-Hua Wang, Ting-Ting Hwang
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(250.18 KB) Additional Information: full citation, references, citings, index terms

5 Characterization of Boolean functions for rapid matching in FPGA technology mapping

U. Schlichtmann, F. Brglez, M. Hermann
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(625.19 KB) Additional Information: full citation, references, citings, index terms

6 On accelerating pattern matching for technology mapping

Yusuke Matsunaga
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**
Publisher: ACM Press
Full text available: pdf(506.73 KB) Additional Information: full citation, references, citings, index terms

7 Sequential optimisation, clocking and Boolean matching: Building a better Boolean matcher and symmetry detector

Donald Chai, Andreas Kuehlmann
March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(236.11 KB) Additional Information: full citation, abstract, references

Boolean matching is a powerful technique that has been used in technology mapping to overcome the limitations of structural pattern matching. The current basis for performing Boolean matching is the computation of a canonical form to represent functions that are equivalent under negation and permutation of inputs and outputs. In this paper, we first present a detailed analysis of previous techniques for Boolean matching. We then describe a novel combination of existing methods and new ideas that ...

8 Combined spectral techniques for Boolean matching

E. Schubert, W. Rosenstiel

February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(243.78 KB) Additional Information: full citation, references, citings, index terms

9 Logic optimization and technology mapping: Technology mapping for low leakage power and high speed with hot-carrier effect consideration

Chang-woo Kang, Massoud Pedram

January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**

Publisher: ACM Press

Full text available: pdf(115.65 KB) Additional Information: full citation, abstract, references

Leakage power and hot-carrier effects are emerging as key concerns in deep sub-micron CMOS technologies with respect to their effects on the total power dissipation and reliability of VLSI circuits. Leakage power dissipation is rapidly becoming a substantial contributor to the total power dissipation as threshold voltage becomes small. Similarly, the hot-carrier effect is one of the most significant failure mechanisms in high-density VLSI circuits. In this paper, a technology mapping technique i ...

10 Improved technology mapping using a new approach to Boolean matching

B. Kapoor

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(539.74 KB) Publisher Site Additional Information: full citation, abstract

We present an improved method for technology mapping using a new approach to the Boolean matching problem. Signatures computed over OBDDs using a set of specific probability values determine matches between library cells and portions of the netlist. Unlike some previous methods, which may require creation of up to O(n!) OBDDs for all possible permutations of module's inputs, our method requires exactly one OBDD to be created for the portion of the netlist being matched. Some results obtained on ...

Keywords: Boolean functions, Boolean matching, ISCAS85 benchmark circuits, OBDDs, circuit optimisation, combinational circuits, computer-aided synthesis, library cells, logic CAD, logic synthesis, probability, specific probability values, technology mapping

11 A spectral method for Boolean function matching

D. M. Miller

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(121.23 KB) Publisher Site Additional Information: full citation, abstract, citings

An approach to Boolean matching with respect to NPN operations, i.e. negation of the function, permutation of the inputs and negation of the inputs, is presented. The method is based on a canonical form defined in the Hadamard spectral domain. When applied to technology mapping, the idea is to keep the canonical function with each library cell, and to compute the canonical function for a subcircuit. The match is then accomplished using hashing on the canonical functions.

Keywords: Boolean function matching, Boolean functions, Hadamard spectral domain, Hadamard transforms, NPN operations, canonical form, hashing, library cell, logic partitioning, negation, permutation, spectral analysis, spectral method, subcircuit, technology mapping

12 Rapid Gate Matching with Don't Cares

A. -M. Trullemans, Q. Zhang

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(638.00 KB) Publisher Site Additional Information: full citation, abstract

Ending the logic synthesis, the technology mapping step maps the Boolean function on physical cells. This itep is based on a matching check, which complexity depends on the number of library cell inputs, and increases if don't cares are considered. The method presented here is based on fault analysis. Using a structural equivalent of the cell, it allows to prune dramatically the design space, and derives at the same time the input phase. The experimental results show a real improvement in CPU ti ...

Keywords: ROBDD, Technology mapping, Boolean matching, Logic synthesis

13 Session 10A: Don't care optimization and boolean matching: Efficient canonical form for boolean matching of complex functions in large libraries

Jovanka Ciric, Carl Sechen

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(357.52 KB) Additional Information: full citation, abstract, references, index terms

A new algorithm is developed which transforms the truth table or implicant table of a Boolean function into a canonical form under any permutation of inputs. The algorithm is used for Boolean matching for large libraries that contain cells with large numbers of inputs and implicants. The minimum cost canonical form is used as a unique identifier for searching for the cell in the library. The search time is nearly constant if a hash table is used for storing the cells' canonical representations i ...

14 Session 32: logic synthesis I: Exploiting K-Distance Signature for Boolean Matching and G-Symmetry Detection

Kuo-Hua Wang

July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**

Publisher: ACM Press

Full text available: pdf(692.56 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present the concept of *k-distance signature* which is a general case of many existing signatures. By exploiting k-distance signature, we propose an *Algorithm for Input Differentiation AID*) which is very powerful to distinguish inputs of Boolean functions. Moreover, based on *AID*, we propose a heuristic method to detect gsym~of Boolean functions and a Boolean matching algorithm. The experimental results show that our methods are not only effective but also ver ...

15 Methods and representations for logic synthesis: A new canonical form for fast boolean matching in logic synthesis and verification

Afshin Abdollahi, Massoud Pedram
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(288.68 KB) Additional Information: full citation, abstract, references, index terms

An efficient and compact canonical form is proposed for the Boolean matching problem under permutation and complementation of variables. In addition an efficient algorithm for computing the proposed canonical form is provided. The efficiency of the algorithm allows it to be applicable to large complex Boolean functions with no limitation on the number of input variables as apposed to previous approaches, which are not capable of handling functions with more than seven inputs. Generalized signatu ...

16 Fast detection of communication patterns in distributed executions
Thomas Kunz, Michiel F. H. Seuren
November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**
Publisher: IBM Press
Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

17 Advances in FPGA CAD: The effect of post-layout pin permutation on timing
Yuzheng Ding, Peter Suaris, Nanchi Chou
February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(327.46 KB) Additional Information: full citation, abstract, references, index terms

In this paper we study the effect of post-layout pin permutation of designs for FPGA devices with non-uniform cell delays. We present a simple, but timing optimal, pin permutation scheme, and report the results of applying the scheme on a set of public logic synthesis benchmark designs that were synthesized and placed by state-of-the-art commercial FPGA design tools configured to maximum optimization level. Despite the preceding optimizations, we still observed an average timing improvement of 3 ...

Keywords: FPGA, logic synthesis, placement, timing optimization

18 An O(N^2) Algorithm for Discovering Optimal Boolean Pattern Pairs
Hideo Bannai, Heikki Hyyro, Ayumi Shinohara, Masayuki Takeda, Kenta Nakai, Satoru Miyano
October 2004 **IEEE/ACM Transactions on Computational Biology and Bioinformatics (TCBB)**, Volume 1 Issue 4
Publisher: IEEE Computer Society Press
Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references

We consider the problem of finding the optimal combination of string patterns, which characterizes a given set of strings that have a numeric attribute value assigned to each string.Pattern combinations are scored based on the correlation between their occurrences in the strings and the numeric attribute values. The aim is to find the combination of patterns which is best with respect to an appropriate scoring function. We present an O(N^2) time algorithm for finding the optimal pair of substrin ...

Keywords: Pattern discovery, Boolean patterns, suffix tree, suffix array.

19 Boolean matching using generalized Reed-Muller forms

Chien-Chung Tsai, Malgorzata Marek-Sadowska
June 1994 **Proceedings of the 31st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(64.43 KB) Additional Information: full citation, references, citings, index terms

20 Statistical profile estimation in database systems

Michael V. Mannino, Paicheng Chu, Thomas Sager
September 1988 **ACM Computing Surveys (CSUR)**, Volume 20 Issue 3
Publisher: ACM Press
Full text available: pdf(2.94 MB) Additional Information: full citation, abstract, references, citings, index terms

A statistical profile summarizes the instances of a database. It describes aspects such as the number of tuples, the number of values, the distribution of values, the correlation between value sets, and the distribution of tuples among secondary storage units. Estimation of database profiles is critical in the problems of query optimization, physical database design, and database performance prediction. This paper describes a model of a database of profile, relates this model to estimating ...

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